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SPECIFICATION

1. Title of the Invention

FILM CARRIER SEMICONDUCTOR DEVICE

2. Claims

(1) A film carrier semiconductor device, comprising: a semiconductor chip in which bumps of conductor projecting parts are mounted on a number of electrode terminals arrayed like a lattice; and

a film carrier tape formed of an insulating tape for placing the semiconductor chip, having carrying and positioning holes arrayed on both sides of the tape and a plurality of device slits provided to expose the respective bumps of every two rows of the semiconductor chip, and provided with a number of leads extended from a number of external connecting terminals provided on the insulating tape corresponding to the respective bumps in the device slits, wherein the respective leads of the film carrier tape and the respective bumps of the semiconductor chip are connected to each other.

(2) The film carrier semiconductor device according to claim 1, wherein the external connecting terminals of the film carrier tape are provided on both sides of the respective device slits.

(3) The film carrier semiconductor device according to claim 1, wherein the film carrier tape has an external lead slit provided in the periphery of the device slit with support parts left at four corners to separate the respective semiconductor chips.

(4) The film carrier semiconductor device according to claim 3, wherein the leads provided on the film carrier tape respectively include an internal lead, one end of which is projected from the upside of the bump into the device slit, an external lead extended from the internal lead to the outside of the external lead slit, and a pad part of an external connecting terminal provided at the tip of the external lead.

(5) The film carrier semiconductor device according to claim 1, claim 2, claim 3 or claim 4, wherein at least the surface of the semiconductor chip is sealed with resin.

3. Detailed Description of the Invention

[Industrial Field of Application]

This invention relates to a film carrier semiconductor device and particularly to the film carrier semiconductor device having a number of leads.

[Prior Art]

According to a manufacturing method of the conventional film carrier semiconductor device, as shown in Fig. 7(a), a film carrier tape 6 in which a metal foil of copper or the like is bonded on an insulation film made of polyimide having a carrying and positioning sprocket hole 1 and a device hole 3 as a hole part where a semiconductor chip 2' enters, and the metal foil is etched to form a lead 4' of a desired shape and a pad 5 for electric selection, and a semiconductor chip 2'

previously provided with a bump 7' which is a metallic projection on the electrode terminal are prepared, and subsequently, the lead 4 of the film carrier tape and the bump 7 of the semiconductor chip are subjected to inner lead bonding by thermo compression method or eutectic method. In the state of the film carrier tape 6, a contact is brought into contact with the upside of the pad 5 for electric selection to perform electric selection or bias test, and subsequently the lead 4 is cut to a desired length. Subsequently, as shown in Fig. 7(b), for example, after the semiconductor chip 2' is fixed on a printed wiring board 8' by an adhesive 9, the lead 4 is bonded to a bonding pad 10 on the printed wiring board by outer lead bonding to complete a semiconductor device.

This type of film carrier semiconductor device manufacturing method, has the advantages that the leads can be bonded all at once regardless of the number of leads to achieve high-speed bonding and that assembling such as bonding and the electric selection work can be automated to attain excellent mass-production.

[Problems that the Invention is to Solve]

In the above conventional film carrier semiconductor device, various problems are caused due to increase in number of electrode terminals and higher processing speed as the capability of the recent semiconductor chip is enhanced in these days.

That is, although the electrode terminals of the semiconductor chip are generally arranged in a line along the peripheral edge of the semiconductor chip, when the number of electrode terminals is large as much as about 300 or more, mostly the size of the semiconductor chip is determined by arranging the electrode terminals so that the size of the semiconductor chip is increased with an increase in number of electrode terminals. Generally the increase in size of the semiconductor chip causes problems such as lowering of yield and information processing speed or increase in packaging density. When the array pitch of the electrodes is made smaller, the above problem is solved, but encountered are some problems such as problem in manufacturing the film carrier tape and problem in accuracy of inner lead bonding, and the reduction in array pitch has a limit. As to the high processing speed of the semiconductor chip or an electronic device loaded with the semiconductor chip, the problem is caused by the delay time due to resistance of the lead connecting the electrode of the semiconductor chip and the bonding pad of the printed wiring board in some case, and particularly as the number of leads is increased, the array pitch of the leads is reduced to decrease the width of the lead, resulting in increase in lead resistance.

The increase in size of the semiconductor chip and the increase in lead resistance sometimes become an irreparable

defect especially to an information processor such as a computer loaded with a number of semiconductor chips or demanded to perform high-speed information processing.

For these problems, as shown in Fig. 8(a) and 8(b), a flip chip bonding method is adopted, in which electrode terminals are formed like a lattice on the surface of a semiconductor chip 2', bumps 7' are mounted on the electrode terminals, the bumps 7' are directly bonded to a bonding pad 10 formed on a printed wiring board. In the case of this flip chip bonding method, the following advantages are obtained. The electrode terminals may arranged not only in the peripheral edge of the semiconductor chip, but also in the whole surface of the semiconductor chip to cope with the increase in number of leads, and further since the electrode terminals of the semiconductor chip and the bonding pad of the printed wiring board are directly bonded to each other, lead resistance is little to cope with high processing speed and also improve the packaging density.

It is, however, general that the semiconductor chip is made of silicon and the printed wiring board is made of ceramics or insulating resin, and silicon and substrate material are different in coefficient of thermal expansion, resulting in the problem that a difference in thermal expansion due to heat generated during the operation of the semiconductor chip greatly exerts influence upon the bonding part to cause cracks

and peel-off in the bonding part. Especially, the high-speed operating semiconductor chip has a large heating value, and also the semiconductor chip is connected only by the bump 7, resulting in the disadvantage that the heat dissipation of the semiconductor is bad. The semiconductor device of multi-electrode terminal in the flip flop bonding has many problems.

It is an object of the invention to solve the problems and provide a film carrier semiconductor device, which may cope with lattice-like array of the electrode terminals and relax a thermal shock to the bonding part by bonding through a lead.

[Means for Solving the Problems]

A film carrier semiconductor device of the invention includes: a semiconductor chip in which bumps of conductor projecting parts are mounted on a number of electrode terminals arrayed like a lattice; and a film carrier tape formed of an insulating tape for placing the semiconductor chip, having carrying and positioning holes arrayed on both sides of the tape and a plurality of device slits provided to expose the respective bumps of the semiconductor chip, and provided with a number of leads extended from a number of external connecting terminals provided on the insulating tape corresponding to the respective bumps in the device slits on both sides of the device slits, wherein the respective leads of the film carrier tape and the respective bumps of the semiconductor chip are

connected to each other.

[Embodiments]

The invention will now be described with reference to the drawings. Fig. 1(a) is a plan view of one embodiment according to the invention, and Fig. 1(b) is a sectional view taken along line A - A' of Fig. 1(a). In the present embodiment, bumps 7 of a semiconductor chip 2 are arrayed like a lattice. A film carrier tape 6 is provided with sprocket holes 1, which are carrying and positioning holes, device slits 11, which are at least two or more and provided like a slit to expose the bump of the semiconductor chip 2, a lead 4, one end of which is projected into the device slit, the other end thereof being provided with an external connecting terminal 12, and a lead slit 14 surrounding the lead 4 and the external connecting terminal 12 with a support part 13 left. The leads 4 of the film carrier tape 6 are connected to the bumps 7 of the semiconductor chip 2.

A manufacturing method of this film carrier semiconductor device will be described.

As shown in the drawing, the film carrier tape 6 in which a metal foil made of copper or the like is bonded on an insulating film having the sprockets 1, which are carrying and positioning holes, the device slits 11, which are at least two or more and provided like a slit to expose the bumps 7 which are electrodes of the semiconductor chip 2, and the lead slits 14 with the

support frame 13 left, the metal foil is etched or the like to form the lead 4 of a desired shape and the external connecting terminal 12, and tin-plating is performed by electroless plating, and the semiconductor chip 2 in which bumps 7 which are metallic projections are previously provided like a lattice on the electrode terminals are prepared, and the leads 4 of the film carrier tape and the bumps 7 of the semiconductor chip are bonded by inner lead bonding.

In this case, the lead 4 of the film carrier tape is projected at one end thereof in the device hole 11, so that the number of lattice-like arrays of the electrodes in the semiconductor chip can be increased by increasing the number of device holes 11. In the inner lead bonding, when a press-bonding tool is provided with a press-bonding part formed to be projected corresponding to the device hole, inner lead bonding can be performed in the same method as before. Further, the external lead-out terminal 12 may be formed like a projection by soldering or the like to facilitate outer lead bonding in the post-process.

Subsequently, the support part 13 of the film carrier tape is cut off, and the semiconductor chip 2 where inner lead bonding is completed is separated from the film carrier tape.

Subsequently, with the surface of the semiconductor chip down as shown in Fig. 2, previously the external connecting terminal 12 of the film carrier tape is bounded to the bonding

pad 10 or the bonding pad 10 of a printed wiring board 8 provided with desired wiring by outer lead bonding to complete the device. At this time, since it is impossible to perform bonding using the conventional press-bonding tool, the projection-like solder provided on the external connecting terminal 12 is fused to perform bonding.

Although the projection-like solder is provided on the external connecting terminal 12 of the film carrier tape in the present embodiment, it may be provided on the bonding pad of the printed wiring board, or on both of them. As the projecting height, about 10 to 50μm is suitable.

Since the tape slit 14 is provided to facilitate cutting off the tape after inner lead bonding, a slit width ranging from 0.5 to 1mm will suffice, and when the film carrier is cut off to surround the lead 4 and the external connecting terminal 12, the tape slit 14 and the support part 13 are unnecessary.

Further, as to the material of the film carrier tape, although it is sufficient that copper foil 35μm thick is bonded to a generally used polyimide film 127μm thick to form a lead, in order to avoid influence upon a connecting part between the external connecting terminal and the bonding pad of the printed wiring board due to a dimensional change caused by thermal expansion or like, it is suitable that the polyimide film is 75 to 100μm thick, and a coefficient of thermal expansion is about equal to or less than 1.5×10^{-6}cm/cm/°C.

Further, as lead plating, tin is suitable because it will facilitate electroless plating, and it is possible that a plating thickness is about 0.3 to 1μm. Electroless gold plating may be similarly performed, and as to the plating thickness, 0.1 to 0.3μm or more is possible.

Fig. 3 is a longitudinal section of a second embodiment of the invention. Similarly to the embodiment 1, bumps 7 are arrayed like a lattice on a semiconductor chip 2, and on the other hand, at least two or more device slits 11 provided like a lit to expose the bumps of the semiconductor chip, a lead 4, one end of which is projected into the device slit 11, the other end thereof being provided with an external connecting terminal 12, and a tape slit 14 surrounding the lead 4 and the external connecting terminal 12 are provided. The lead 4 of a film carrier tape is connected to the bump 7 of the semiconductor chip. Further, resin 15 is sealed up to cover the surface of the semiconductor chip at least.

A manufacturing method of the above film carrier semiconductor device will now be described. Similarly to the embodiment 1, as shown in Figs. 1(a), 1(b), the film carrier tape 6 in which a metal foil made of copper or the like is bonded on an insulating film having the sprocket holes 1, which are carrying and positioning holes, the device slits 11, which are at least two or more and provided like a slit to expose the bumps which are electrodes of the semiconductor chip 2, and

the lead slits 14 with the support frame 13 left, the metal foil is etched or the like to form the lead of a desired shape and the external connecting terminal 12, and tin-plating is performed by electroless plating, and the semiconductor chip 2 in which bumps 7 which are metallic projections are previously provided like a lattice on the electrode terminals are prepared, and the leads 4 of the film carrier tape and the bumps 7 of the semiconductor chip are bonded by inner lead bonding.

Subsequently, as shown in Fig. 3, resin 15 is sealed up to cover the surface of the semiconductor chip at least. As the resin, liquid resin such as epoxy resin or silicon resin is used, and when the resin is dripped from the device slit 14, the surface of the semiconductor chip can be easily covered and sealed.

Subsequently, similarly to the embodiment 1, the support part 13 of the film carrier tape is cut off to separate the semiconductor chip 2 from the film carrier tape, and as shown in Fig. 3, with the chip surface down, the bonding pad 10 of the printed wiring board 8 and the external connecting terminal 12 of the film carrier tape are bonded by outer lead bonding to complete the device.

In this case, in the second embodiment, since the surface of the semiconductor chip 2 is sealed with resin, the reliability such as moisture resistance is improved, besides the mechanical strength can be increased, which leads to the

advantage that when outer lead bonding is performed to the printed wiring board with the surface down, even if load is applied from the back of the semiconductor chip, the film provided with the external connecting terminal located at the semiconductor surface can be bonded without deformation to attain high-reliability bonding. As the resin thickness, about 10 to 20μm is enough, but in order to obtain satisfactory mechanical strength, preferably the thickness has such a range that the gap between the semiconductor chip and the film located on the semiconductor chip is filled up with resin, and also not to exceed the height of the external connecting terminal on the tape carrier film, so about 50 to 120μm is suitable.

Figs. 4(a) and 4(b) are a plan view of a third embodiment of the invention and a sectional view taken along line A - A' thereof. In present embodiment, a lead is different in structure from the embodiment 1, and the lead 20 is provided with an internal lead 21, one end of which is projected into a device slit 11, the other end thereof being provided with an external lead 22 extended from the internal lead 21 beyond an external lead slit 14 and an electric selection pad 23 of an external connecting terminal at the end.

In the present embodiment, as shown in Figs. 4(a) and 4(b), a metal foil made of copper or the like and 18 to 50μm thick is bonded on an insulating film having sprockets 1, which are carrying and positioning holes, the device slits 11, which

are at least two or more and provided like a slit to expose the bumps 7, and the external lead slits 14 with a support frame 13 and made of polyimide or the like with a thickness of 50 to 125μm, and the metal foil is etched or the like to form the lead 20 of a desired shape. The lead 20 is provided with an internal lead 21, an external lead 22, and an electric selection pad 23. Further, the lead 20 is plated 0.5 to 5μm thick with gold or tin by electroless plating or electrolytic plating to complete a film carrier tape 6. In the case of plating by an electrolytic plating method, a leading wiring for plating is provided from the electric selection pad 23 to perform that plating.

Subsequently, the internal leads 4 of the film carrier tape 6 and the bumps 7 of the metallic projections previously provided like a lattice on the electrode terminals of the semiconductor chip 2 are bonded, and a contact is brought into contact with the electric selection pad 23 to perform electric selection and bias test. Thus, a film carrier semiconductor device is completed.

In this case, one end of the internal lead 21 of the film carrier tape is projected into the device slit 11, so that the number of lattice-like arrays of electrodes of the semiconductor chip can be increased by increasing the number of the device slits 11.

In the packaging method of the present embodiment, the

support part 13 of Fig. 4 is cut off, and the external lead 22 is cutoff and formed in the vicinity of the outer peripheral edge of the external lead slit 14 to separate the semiconductor device from the film carrier tape as shown in Fig. 5(a). Subsequently, as shown in Fig. 5(b), with the surface of the semiconductor chip 2 down, previously an external lead 12 of the film carrier semiconductor device is bonded to a bonding pad 10 or a bonding pad of a printed wiring board 8 provided with desired wiring by outer lead bonding to complete the device.

Although packaging is performed to the printed wiring board with the chip surface down in the present embodiment, it is also possible to perform packing with the surface up by making the external lead 22 enough long and forming the same into a desired shape.

Fig. 6(a) is a longitudinal section of a fourth embodiment of the invention. Although the present embodiment has the same structure as the third embodiment, an internal lead 21 of a film carrier tape 6 is connected to a bump 7 of a semiconductor chip 2 with the surface of a lead 20 of the film carrier tape down conversely to the third embodiment, and further, similarly to the second embodiment, resin 15 is sealed up to cover the surface of the semiconductor chip 2 at least.

In a manufacturing method of the present embodiment, similarly to the third embodiment, the film carrier tape 6 and

the semiconductor chip 2 provided with the bumps 7 like a lattice on the electrode terminals are prepared, and as shown in Fig. 6(a), with the lead 20 surface of the film carrier tape down, the internal lead 21 and the bump 7 of the semiconductor chip 2 are bonded by inner lead bonding. Subsequently, similarly to the second embodiment, resin 15 is sealed up to cover the surface of the semiconductor chip 2 at least. In this case, a contact is brought into contact with the upside of the electric selection pad 23 to perform electric selection or a bias test. Thus, the film carrier semiconductor device is completed.

As to a packaging method, similarly to the third embodiment, a support part 13 is cut off, and an external lead 22 is cut off and formed in the vicinity of the outer edge of an external lead slit to separate the semiconductor device form the film carrier tape 6. After that, as shown in Fig. 6(b), with the surface of the semiconductor chip 2 down, previously the external lead 22 of the film carrier semiconductor device is bonded to a bonding pad 10 or a bonding pad 10 of a printed wiring board 8 provided wit desired wiring by outer lead bonding. Similarly to the third embodiment, with the surface up, packaging to the printed wiring board can be performed.

In the present embodiment, the film carrier tape is located between the lead 15 of the film carrier tape 6 and the bonding pad 10 or the wiring of the printed wiring board 8,

whereby short-circuit between the lead 20, the bonding pad 10 and the wiring can be completely prevented, and further the reliability such as moisture resistance can be improved and mechanical strength can be increased by resin sealing. Therefore, in the process of handling or packaging to the printed wiring board, it is possible to prevent deformation or the like of the lead and the film tape part located on the surface of the semiconductor chip. As the thickness of the resin 15, about 10 to 20μm may be enough, but in order to attain the satisfactory mechanical strength, preferably the range is such that the space between the semiconductor chip 2 and the part of the film tape 6 is filled up with resin, so about 50 to 300μm is suitable.

[Advantage of the Invention]

According to the invention, as described above, the semiconductor chip having the electrode terminals arrayed like a lattice suitable for multi-electrode is adopted to relax the limit in number of arrayed electrode terminals caused in the conventional film carrier semiconductor device and enable multi-electrode, and as to the problem such as cracks and peel off in the bonding part due to a difference in thermal expansion between the semiconductor chip and the printed wiring board, which has been caused in the conventional flip chip bonding in which the semiconductor chip where the electrode terminals are arrayed like a lattice is directly bonded with the surface

down to the semiconductor chip, the invention has the effect of remarkably relaxing the problem by the leads. Further the connection to the printed wiring board is made in the vicinity of the electrode terminals on the semiconductor chip to minimize the length of the lead so that the electric resistance of the lead can be held down to the minimum, which leads to the advantage of being suitable for high-speed information processing.

As to the lead resistance between the semiconductor chip and the printed wiring board, although it is disadvantageous that the lead is longer as compared with the flip chip bonding, as compared with the case of wiring in the semiconductor chip and providing the electrode terminals on the semiconductor chip edge as in the conventional film carrier semiconductor device, in the invention, wiring is made by the leads of the film carrier tape so that lead resistance can be remarkably reduced as compared with the conventional film carrier semiconductor device to attain high-speed processing.

4. Brief Description of the Drawings

Figs. 1(a) and (b) are a plan view of one embodiment of a film carrier semiconductor device according to the invention, and a sectional view taken along A - A' thereof;

Fig. 2 is a longitudinal section showing an example of packaging the film carrier semiconductor device of the present

embodiment;

Fig. 3 is a longitudinal section of a second embodiment according to the invention;

Figs. 4(a) and (b) are a plan view of a third embodiment according to the invention and a sectional view taken along line A - A' thereof;

Figs. 5(a) and (b) are sectional views showing the process of packaging the third embodiment and the packaged state thereof;

Figs. 6(a) and (b) are sectional views showing a fourth embodiment of the invention and the packaged state thereof;

Figs. 7(a) and (b) are a plan view of an example of the conventional film carrier semiconductor device and a longitudinal section of the packaged state thereof; and

Figs. 8(a) and (b) are a plan view of the general film carrier semiconductor device and a longitudinal section of the packaged state thereof.

1: sprocket hole 2, 2': semiconductor chip 3: device hole 4, 4', 20: lead 5, 23: selection pad 6: film carrier tape 7, 7': bump 8, 8': printed wiring board 9: adhesive 10: bonding pad 11: device slit 12: external connecting terminal 13: support part 14: tape slit 15: resin 21: internal lead 22: external lead

FIGURE 1(A)

1: SPROCKET HOLE

2: SEMICONDUCTOR CHIP

4: LEAD

6: FILM CARRIER TAPE

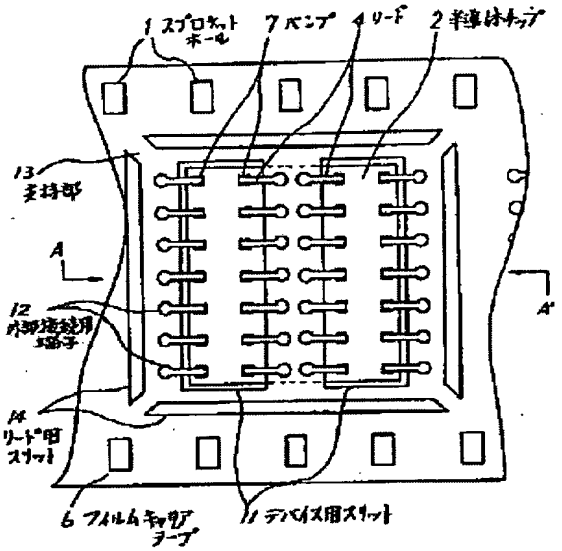
7: BUMP

11: DEVICE SLIT

12: EXTERNAL CONNECTING TERMINAL

13: SUPPORT PART

14: LEAD SLIT



第 1 図 (a)

FIGURE 1(B)

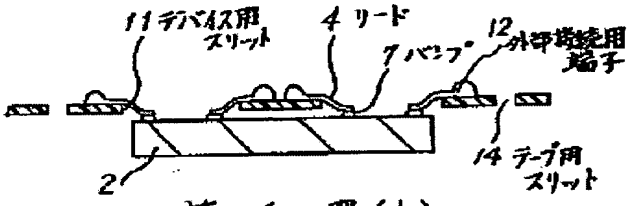
4: LEAD

7: BUMP

11: DEVICE SLIT

12: EXTERNAL CONNECTING TERMINAL

14: TAPE SLIT



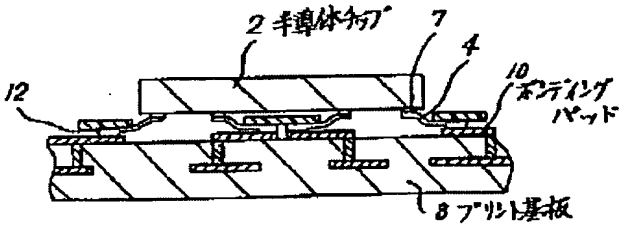
第 1 図 (b)

FIGURE 2

2: SEMICONDUCTOR CHIP

8: PRINTED WIRING BOARD

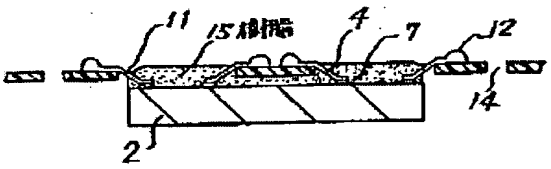
10: BONDING PAD



第 2 図

FIGURE 3

15: RESIN



第 3 図

FIGURE 4(A)

2: SEMICONDUCTOR CHIP

6: FILM CARRIER TAPE

7: BUMP

11: DEVICE SLIT

13: SUPPORT PART

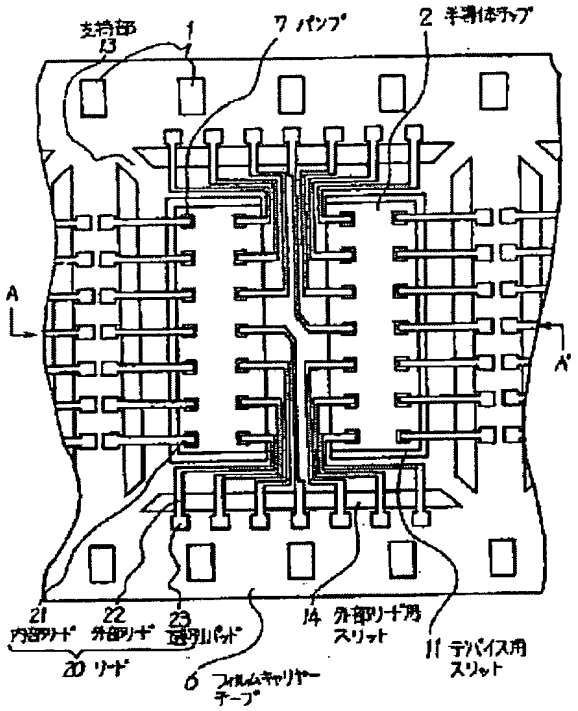
14: EXTERNAL LEAD SLIT

20: LEAD

21: INTERNAL LEAD

22: EXTERNAL LEAD

23: SELECTION PAD



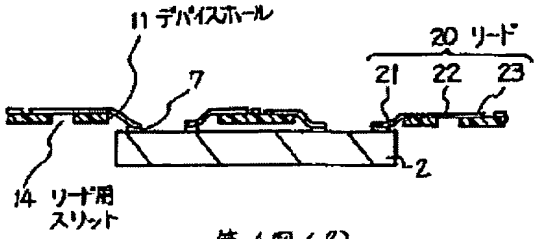
第 4 図 (a)

FIGURE 4(B)

11: DEVICE HOLE

14: LEAD SLIT

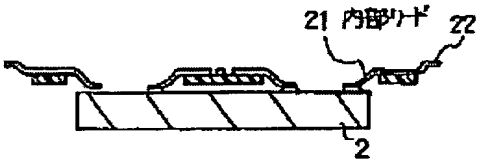
20: LEAD



第 4 図 (b)

FIGURE 5(A)

21: INTERNAL LEAD



第 5 図 (a)

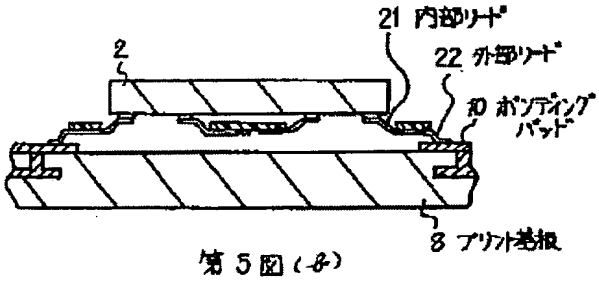
FIGURE 5(B)

8: PRINTED WIRING BOARD

10: BONDING PAD

21: INTERNAL LEAD

22: EXTERNAL LEAD



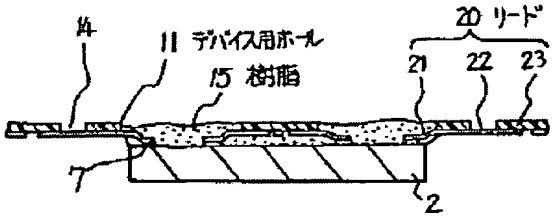
第 5 図 (b)

FIGURE 6(A)

11: DEVICE HOLE

15: RESIN

20: LEAD



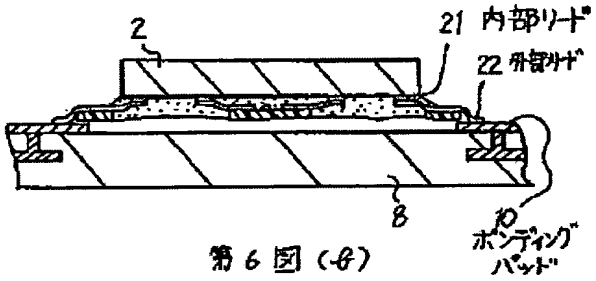
第6図(a)

FIGURE 6(B)

10: BONDING PAD

21: INTERNAL LEAD

22: EXTERNAL LEAD



第6図(B)

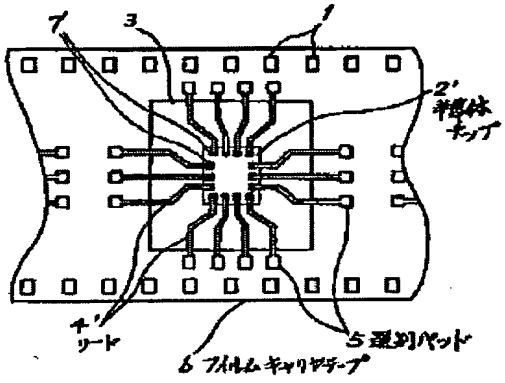
FIGURE 7(A)

2': SEMICONDUCTOR CHIP

4': LEAD

5: SELECTION PAD

6: FILM CARRIER TAPE



第7図(a)

FIGURE 7(B)

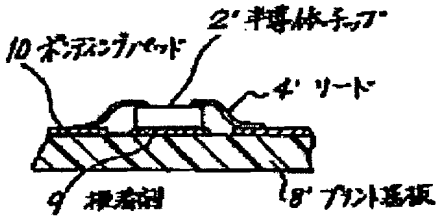
2': SEMICONDUCTOR CHIP

4': LEAD

8': PRINTED WIRING BOARD

9: ADHESIVE

10: BONDING PAD

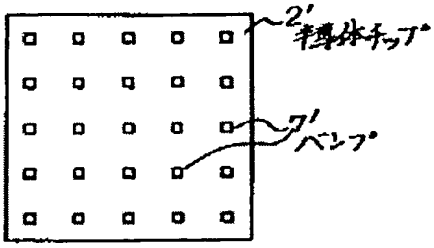


第7図(b)

FIGURE 8(A)

2′: SEMICONDUCTOR CHIP

7′: BUMP

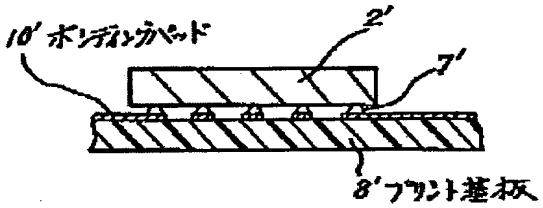


第 8 図 (a)

FIGURE 8(B)

8′: PRINTED WIRING BOARD

10′: BONDING PAD



第 8 図 (b)